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(FILE 'USPAT' ENTERED AT 14:25:49 ON 16 APR 1998)
L1            30 S ISOCHRONOUS CHANNEL
L2            14 S L1 AND BUFFERS
L3             5 S L2 AND LIST
L4             2 S L3 AND ADDING
L5             2 S L4 AND DATA (P) PATH
L6             2 S L5 AND SEND
L7             2 S L6 AND NODE
L8             2 S L7 AND ISOCHRONOUS (P) DATA

=> d 1-
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1. 5,668,811, Sep. 16, 1997, Method of maintaining frame synchronization in a communication network; Debra J. Worsley, et al., 370/424, 506 [IMAGE AVAILABLE]

2. 5,566,169, Oct. 15, 1996, Data communication network with transfer port, cascade port and/or frame synchronizing signal; Geetha N. K. Rangan, et al., 370/366, 352, 426 [IMAGE AVAILABLE]

L9	287	S	395/287/CCLS
L10	287	S	395/287?/CCLS
L11	27	S	CONFIGUR? (5A) ISOCHRONOUS
L12	343	S	LINKED LIST (P) BUFFER#
L13	1	S	L9 AND L12
L14	1	S	L10 AND L12
L15	3	S	L12 AND ISOCHRONOUS
L16	2	S	L15 AND CONFIGUR?
L17	2	S	L16 AND PATH
L18	1	S	L17 AND SENDER

=> d l14

1. 5,434,976, Jul. 18, 1995, Communications controller utilizing an external buffer memory with plural channels between a host and network interface operating independently for transferring packets between protocol layers; Min P. Tan, et al., 395/200.64; 364/228.5, 239, 239.7, DIG.1; 395/200.43, 200.8, **287**, 846, 847; 711/1, 149 [IMAGE AVAILABLE]

=> d l17 1-

1. 5,812,800, Sep. 22, 1998, Computer system which includes a local expansion bus and a dedicated real-time bus and including a multimedia memory for increased multi-media performance; Dale E. Gulick, et al., 395/308, 281, 306, 309, 822, 842, 847, 856, 857 [IMAGE AVAILABLE]

2. 5,754,789, May 19, 1998, Apparatus and method for controlling point-to-point interconnect communications between nodes; Andreas G. Nowatzyk, et al., 395/200.63, 182.1, 200.67, 200.68, 200.78 [IMAGE AVAILABLE]

=> d

1. 5,754,789, May 19, 1998, Apparatus and method for controlling point-to-point interconnect communications between nodes; Andreas G. Nowatzyk, et al., 395/200.63, 182.1, 200.67, 200.68, 200.78 [IMAGE AVAILABLE]

SUMMARY:

BSUM(10)

Other problems to contend with include the need to prioritize certain types of data transfers. **Isochronous** data transfers for real-time information such as video and sound may not be unduly delayed and must be delivered in. . .

SUMMARY:

BSUM(17)

It is another object of the present invention to provide priorities for data packets thus enabling **Isochronous** data transfers for real-time information.

SUMMARY:

BSUM(22)

These . . . being inserted when no other information is being transferred. The delay time in transmission is adjusted by a temporal alignment **buffer** in the channel modules to ensure that an integral multiple of packet transmission times are used for the total delay. . . arrival and start of each packet transmission. The four channel modules on a single interconnect controller chip share a common **buffer** pool with **linked list** entries for identifying which channel module is to propagate each received packet. The common **buffer** pool is segmented into sixteen (16) bit segments so that received packets may begin retransmission before completing arrival. This also. . .

DRAWING DESC:

DRWD(5)

FIGS. 3(a)-3(b) illustrate **configurations** of multiple interconnect controllers to form larger switches in accordance with the present invention.

DETDESC:

DETD(7)

In . . . to the I/O circuit 101 for providing communications between computer 100 and adjacent nodes on the network though certainly alternative **configurations** may be appropriate.

DETDESC:

DETD(13)

Before . . . data packets exchanged between nodes in accordance with the preferred embodiment of the present invention. FIG. 4 illustrates an arbitrarily **configured** collection of seven nodes. The dark lines between nodes indicate point-to-point interconnections between nodes, connected to one of the serial. . .

DETDESC:

DETD(15)

FIG. . . . monitoring routines. There are a number of methods known for computing the routing tables such as those implementing the shortest **path** solutions suggested by a number of conventional textbooks. The operation of the present invention will be described assuming accurately filled. . .

DETDESC:

DETD(27)

When a channel module attempts to write received data into the packet **buffer** pool, the 12-bit address is simultaneously supplied to the routing table circuitry 29. The routing table circuitry outputs an 8-bit word that specifies which virtual channel may be used for the packet. This word is interpreted by the **buffer** control logic 41. The **buffer** control logic 41 maintains a **linked list** index to the registers of the packet **buffer** pool. Various registers may be free or occupied at different times irrespective of their actual location in the register file. The **linked list** index provides head-to-tail **linked list** pointers for all stored data packets and is used to index the packet **buffer** pool 40. By using the multi-ported register file that is accessible by all channels, each channel module may deposit received. . .

DETDESC:

DETD(30)

At . . . with two virtual channels each. A set bit in the virtual channel mask designates the corresponding channel module as a **path**. The least significant 4 bits specify virtual channel 0 while the most significant 4 bits specify virtual channel 1 and. . .

DETDESC:

DETD(34)

A . . . in integral multiple of the packet transmission time. This is achieved by adding the delay element in the receive data **path**, which is essentially a 16-bit wide shift register of depth 0-5. The depth is set during the initialization procedure when. . .

DETDESC:

DETD(40)

A . . . a channel module due to lack of buffers or a corrupted packet are placed in a reject queue by the **sender**. Rejected packets go through a routing cycle to determine a new transmit channel and are then inserted at the head. . .

DETDESC:

DETD(53)

Another . . . will wake it up to an accessible state after a predetermined amount of time. This facility also provides for remote **configuration** of interconnect controllers.

CLAIMS:

CLMS(1)

We . . .
of said data packet;
appending said data packet with said check code bits; and
continuously conveying data packets between adjacent nodes through **isochronous** coupled communications channels by conveying a data packet upon receiving a data packet.

CLAIMS:

CLMS(2)

2. . . .
said adjacent nodes, said coupled channel modules of two adjacent nodes continuously exchanging a flow of data packets through an **isochronous** communications channel;
timing control logic means incorporated in each of said plurality of channel modules for adjusting the round trip delay. . .

CLAIMS:

CLMS(6)

6. . . .
said adjacent nodes, said coupled channel modules of two adjacent nodes continuously exchanging a flow of data packets through an **isochronous** communications channel;
timing control logic means incorporated in each of said plurality of channel modules for adjusting the round trip delay. . .